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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,127	04/01/2004	Sung-Ho Kang	P4068/PSM	8047

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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	**PAPER NUMBER**
2117	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/814,127	KANG ET AL.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because: the inventor Guen-Bae Kim did not mention the date of signature.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1, 3, 4, 5, 8, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120) in view of Chen et al. (Efficient BIST TPG Design and Test Set Compaction via Input Reduction, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Vol. 17, No. 8, August 1998, Pages 692-705), Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464), Okada et al. (US 5,796,356) and Liau et al. (US 6,574,280 B1).

As per claim 1, Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding) teach a test data compression method comprising steps of: (b) generating a compression code based on a statistical coding ("The compression/decompression scheme described in this paper is based on statistical coding", page 115, col. 1, paragraph 6; Jas et al. "Given the test set for a core, a statistical code for compressing the test set must be selected", page 117, col. 2, paragraph 4, Jas et al. "An example to illustrate the proposed approach for selecting a statistical code is shown in Fig. 3", page 118, col. 2, paragraph 2, Jas et al.); (c) replacing unspecified bits ('X' values) of the test data with specific values chosen to maximize compression of the test data ("When encoding a block containing X's, the value of X's can be chosen to match the codeword whose representation requires the smallest number of bits", page 119, col. 2, paragraph 1, Jas et al.); and (e) compressing the blocks using the compression code ("the compression/decompression scheme described in this paper is based on statistical coding", page 115, col. 1, paragraph 6, Jas et al.) wherein the compression code is generated in such a manner that only one recurring 4-bit pattern that has the highest frequency of appearance is compressed ("Consider the test set in Fig. 1. If we divide the entire test set into 4-bit blocks then we get the frequency distribution as shown in the second column of Table 1. As can be seen from Table 1, the patterns having the highest frequencies are 0010, 0100 and 0110. So these are the patterns that are coded while the rest of them will be left unchanged", page 118, col. 2, paragraph 2, Jas et al.)

However Jas et al. do not explicitly teach (a) finding compatible inputs and inversely compatible inputs using given test data TD.

Chen et al. in an analogous art teach that input reduction is based on new concepts of compatibility and inverse compatibility, which can be used to identify circuit inputs that can be combined into test signals without reducing fault coverage (page 693, col. 1, paragraph 5, Chen et al.). Chen et al. also teach "Definition 1 (Compatible Inputs): If all detectable target faults in a circuit C remain detectable in the circuit Ci-j, obtained by combining inputs x_i and x_j of C into a test signal, then x_i and x_j are said to be compatible", (page 694, col. 1, paragraph 5, Chen et al.). Chen teach "Definition 2 (Inversely Compatible Inputs): If all detectable target faults in a circuit C remain detectable in the circuit $Ci \cong j$, obtained by combining inputs x_i

and x_j of C into a test signal via an inverter, then x_i and x_j are said to be inversely compatible", (page 694, col. 1, paragraph 7, Chen et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jas et al.'s publication with the teachings of Chen et al. by including an additional step of finding compatible inputs and inversely compatible inputs using given test data TD.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to combine circuit inputs into test signals without reducing fault coverage.

Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120) also do not explicitly teach (d) re-ordering a sequence of patterns of the test data to generate as many instances as possible of the bit pattern to be compressed based on the size of the blocks.

However Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464) in an analogous art teach ordering the test vectors in the test set such that correlated test vectors follow each other results in difference vectors with many more 0's than 1's (page 460, col. 1, paragraph 3, Jas et al.). Jas et al. also teach that the minimum cost path through the graph that does not repeat any vectors corresponds to the optimum ordering of the test vectors to maximize the compression (page 460, col. 2, paragraph 4, Jas et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120) publication with the teachings of Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464) by including an additional step of (d) re-ordering a sequence of patterns of the test data to generate as many instances as possible of the bit pattern to be compressed based on the size of the blocks.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to maximize the compression of test data bits.

Jas et al. also do not explicitly teach that the pattern that has the highest frequency of appearance is compressed into a 1-bit compression code.

However Okada et al. in an analogous art teach that from the states of FIGS. 30 and 31, the symbol "a" occurs 18 times, and when its occurrence frequency amounts to "25", the state of the code tree becomes as illustrated in FIG. 33. In this code tree, as depicted in FIG. 33, "a" can be compressed down to 1 bit (fig. 33, col. 3, lines 29-33, Okada et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jas et al.'s publication with the teachings of Okada et al. by including additionally that the pattern that has the highest frequency of appearance is compressed into a 1-bit compression code.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce the number of data bits and reduce data processing and transmission time.

Jas et al. also do not explicitly teach that the other bits are grouped into blocks consisting of a 2-bit codeword, the 2-bit codeword blocks having the original values of the bits.

However Liau et al. in an analogous art teach that in contrast to conventional pulse code modulation (PCM) systems that transmit 8-bit codewords at 8 kHz, ADPCM compression techniques enable the data to be transmitted in the form of 4-bit, 3-bit, or 2-bit codewords at 8kHz (col. 1, lines, 43-48, Liau et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jas et al.'s publication with the teachings of Liau et al. by including additionally that the other bits are grouped into blocks consisting of a 2-bit codeword, the 2-bit codeword blocks having the original values of the bits.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to reduce the bandwidth of the transmitted signal and to improve the quality of data transmission.

- As per claim 3, Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120), Chen et al. (Efficient BIST TPG Design and Test Set Compaction via Input Reduction, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Vol. 17, No. 8, August 1998, Pages 692-705), Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464), Okada et al. (US 5,796,356) and Liau et al. (US 6,574,280 B1) teach the additional limitations.

Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120) teach that the step (c) replaces all the 'X' values with 'O's such that the patterns have a lot of 'O's ("When encoding a block containing X's, the value of X's can be chosen to match the codeword whose representation requires the smallest number of bits", page 119, col. 2, paragraph 1, Jas et al.) and using the compression code generated in the step (b), ("The compression/decompression scheme described in this paper is based on statistical coding", page 115, col. 1, paragraph 6, Jas et al.).

Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464) teach that the step (d) includes a step of storing the first value and the last value of each test data pattern in which 'X' values have been replaced with 'O's and previously calculating the length of the pattern and a step of making the last value of each pattern become identical to a value of the next pattern and re-ordering the sequence of the patterns to generate as many instances as possible of the block to be compressed, so that a block having consecutive 'O's can frequently appear ("By carefully ordering the test vectors in the test set, the number of 0's in the difference vectors can be maximized. Test vectors tend to be correlated. Thus, many pairs of test vectors in the test set will have similar input combinations such that the difference vectors have a lot of 0's. Ordering the test vectors in the test set such that correlated test vectors follow each other results in difference vectors with many more 0's than 1's", page 460, col. 1, paragraph 3, Jas et al.).

Okada et al. teach that the step (e) selects and compresses one block having the highest frequency of appearance (fig. 33, col. 3, lines 29-33, Okada et al.).

- As per claim 4, Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120), Chen et al. (Efficient BIST TPG Design and Test Set Compaction via Input Reduction, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Vol. 17, No. 8, August 1998, Pages 692-705), Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464), Okada et al. (US 5,796,356) and Liau et al. (US 6,574,280 B1) teach the additional limitations.

Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120) teach a test data decompression apparatus including a controller that decompresses test data compressed by the test data compression method as claimed in claim 1, inputs the decompressed test data to a scan chain in the tested device, and controls signals transmitted between an ATE and an FSM, comprising: an FSM decoder that includes inputs, one of which is a test clock input and the other an input to which the compressed test data is transmitted from a channel of a tester, and outputs, one of which is a data output port through which original data obtained when the compressed data is decompressed is transmitted and the other an output port through which control signals are output; and a serializer that inputs the decompressed test data to the scan chain in synchronization with an FSM clock of the FSM decoder and a chip test clock ("The compression/decompression scheme...slow tester", Fig. 4, page 116, col. 2, paragraphs 2-3, "One way to implement the decoder...into the serializer", page 119, col. 1, paragraph 1, Jas et al.).

- As per claim 5, Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120), Chen et al. (Efficient BIST TPG Design and Test Set Compaction via Input Reduction, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Vol. 17, No. 8, August 1998, Pages 692-705), Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to

Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464), Okada et al. (US 5,796,356) and Liau et al. (US 6,574,280 B1) teach the additional limitations.

Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120) teach that the control signals include a signal "parallel load (Par.)", a signal "serial load (Ser.)" and a signal "Wait", when the first bit of the compression bit is ' 1', which represents an uncompressed pattern, the decoder transmits subsequent bits and the control signal "serial load (Ser.)" to the serializer for two clock cycles, and when the first bit of the compression bit is '0', which indicates one compressed block, the decoder delivers P0 corresponding to bits of the corresponding block and the control signal "parallel load(Par.)" in parallel to the serializer ("Each time the decoder is clocked once, the scan chain is clocked n times", Fig. 4, page 117, col. 1, paragraph 1, "One way to implement the decoder...shown in Fig. 6", page 119, col. 1, paragraphs 1, 2, Jas et al.). The examiner would like to point out that it is obvious to one of ordinary skill in the art at the time the invention was made to implement a control signal "Wait" for the decoder for loading data into the serializer.

- As per claim 8, Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120), Chen et al. (Efficient BIST TPG Design and Test Set Compaction via Input Reduction, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Vol. 17, No. 8, August 1998, Pages 692-705), Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464), Okada et al. (US 5,796,356) and Liau et al. (US 6,574,280 B1) teach the additional limitations.

Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120) teach a test data decompression apparatus including a controller that decompresses test data compressed by the test data compression method as claimed in claim 3, inputs the decompressed test data to a scan chain in the tested device, and controls

signals transmitted between an ATE and an FSM, comprising: an FSM decoder that includes inputs, one of which is a test clock input and the other an input to which the compressed test data is transmitted from a channel of a tester, and outputs, one of which is a data output port through which original data obtained when the compressed data is decompressed is transmitted and the other an output port through which control signals are output; and a serializer that inputs the decompressed test data to the scan chain in synchronization with an FSM clock of the FSM decoder and a chip test clock ("The compression/decompression scheme...slow tester", Fig. 4, page 116, col. 2, paragraphs 2-3, "One way to implement the decoder...into the serializer", page 119, col. 1, paragraph 1, Jas et al.).

- As per claim 9, Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120), Chen et al. (Efficient BIST TPG Design and Test Set Compaction via Input Reduction, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Vol. 17, No. 8, August 1998, Pages 692-705), Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464), Okada et al. (US 5,796,356) and Liau et al. (US 6,574,280 B1) teach the additional limitations.

Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120) teach that the control signals include a signal "parallel load (Par.)", a signal "serial load (Ser.)" and a signal "Wait", when the first bit of the compression bit is '1', which represents an uncompressed pattern, the decoder transmits subsequent bits and the control signal "serial load (Ser.)" to the serializer for two clock cycles, and when the first bit of the compression bit is '0', which indicates one compressed block, the decoder delivers P0 corresponding to bits of the corresponding block and the control signal "parallel load(Par.)" in parallel to the serializer ("Each time the decoder is clocked once, the scan chain is clocked n times", Fig. 4, page 117, col. 1, paragraph 1, "One way to implement the decoder...shown in Fig. 6", page 119, col. 1, paragraphs 1, 2, Jas et al.). The examiner would like to point out that it is obvious to one of ordinary skill in the art at the

time the invention was made to implement a control signal "Wait" for the decoder for loading data into the serializer.

5. Claims 2, 6, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120), Chen et al. (Efficient BIST TPG Design and Test Set Compaction via Input Reduction, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Vol. 17, No. 8, August 1998, Pages 692-705), Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464), Okada et al. (US 5,796,356) and Liau et al. (US 6,574,280 B1) as applied to claim 1 above, and further in view of Koenemann et al. (US 5,612,963).

As per claim 2, Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120), Chen et al. (Efficient BIST TPG Design and Test Set Compaction via Input Reduction, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Vol. 17, No. 8, August 1998, Pages 692-705), Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464), Okada et al. (US 5,796,356) and Liau et al. (US 6,574,280 B1) substantially teach the claimed invention described in claim 1 (as rejected above).

Chen et al. further teach that the step (a) comprises the steps of: preparing an input check set C and initializing C_i ($0 <= i <= N-1$) to UNIQUE (UNIQUE means that an input i is not compatible or inversely compatible); detecting compatibility between an input v(i,k) and a comparison input v(j,k) over the entire test sequence k ($0 <= k <= L-1$) of the given test data TD using a function is compatible; and compatible inputs or inversely compatible inputs ("Based on the complete test set...inversely compatible", page 694, col. 1, paragraphs 3-7, Chen et al.).

However Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120), Chen et al. (Efficient BIST TPG Design and Test Set Compaction via Input Reduction, IEEE Transactions on Computer-aided Design of

Integrated Circuits and Systems, Vol. 17, No. 8, August 1998, Pages 692-705), Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464), Okada et al. (US 5,796,356) and Liau et al. (US 6,574,280 B1) do not explicitly teach confirming whether there are values that conflict with previous other inputs using a function conflict check if the input v(i, k) or v(j, k) has an 'X' value (don't care).

Koenemann et al. in an analogous art teach that any conflicting and "don't care" input requirements are assigned a weight value of ½ (table 1, page 5, lines 63-64, Koenemann et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Jas et al.'s publication with the teachings of Koenemann et al. by including an additional step of confirming whether there are values that conflict with previous other inputs using a function conflict check if the input v(i, k) or v(j, k) has an 'X' value (don't care).

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to determine the conflicting inputs.

- As per claim 6, Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120), Chen et al. (Efficient BIST TPG Design and Test Set Compaction via Input Reduction, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Vol. 17, No. 8, August 1998, Pages 692-705), Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464), Okada et al. (US 5,796,356), Liau et al. (US 6,574,280 B1) and Koenemann et al. teach the additional limitations.

Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120) teach a test data decompression apparatus including a controller that decompresses test data compressed by the test data compression method as claimed in claim 2, inputs the decompressed test data to a scan chain in the tested device, and controls

signals transmitted between an ATE and an FSM, comprising: an FSM decoder that includes inputs, one of which is a test clock input and the other an input to which the compressed test data is transmitted from a channel of a tester, and outputs, one of which is a data output port through which original data obtained when the compressed data is decompressed is transmitted and the other an output port through which control signals are output; and a serializer that inputs the decompressed test data to the scan chain in synchronization with an FSM clock of the FSM decoder and a chip test clock ("The compression/decompression scheme...slow tester", Fig. 4, page 116, col. 2, paragraphs 2-3, "One way to implement the decoder...into the serializer", page 119, col. 1, paragraph 1, Jas et al.).

- As per claim 7, Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120), Chen et al. (Efficient BIST TPG Design and Test Set Compaction via Input Reduction, IEEE Transactions on Computer-aided Design of Integrated Circuits and Systems, Vol. 17, No. 8, August 1998, Pages 692-705), Jas et al. (Test Vector Decompression via Cyclical Scan Chains and Its Application to Testing Core-Based Designs, International Test Conference, Oct. 1998, Proceedings, Pages: 458-464), Okada et al. (US 5,796,356), Liau et al. (US 6,574,280 B1) and Koenemann et al. teach the additional limitations.

Jas et al. (Scan Vector Compression/Decompression Using Statistical Coding, VLSI Test Symposium, April 1999, Proceedings, 17th IEEE, Pages 114-120) teach that the control signals include a signal "parallel load (Par.)", a signal "serial load (Ser.)" and a signal "Wait", when the first bit of the compression bit is ' 1', which represents an uncompressed pattern, the decoder transmits subsequent bits and the control signal "serial load (Set.)" to the serializer for two clock cycles, and when the first bit of the compression bit is '0', which indicates one compressed block, the decoder delivers P0 corresponding to bits of the corresponding block and the control signal "parallel load(Par.)" in parallel to the serializer ("Each time the decoder is clocked once, the scan chain is clocked n times", Fig. 4, page 117, col. 1, paragraph 1, "One way to implement the decoder...shown in Fig. 6", page 119, col. 1, paragraphs 1, 2, Jas et al.). The examiner would like to point out that it is obvious to one of ordinary skill in the art at the

time the invention was made to implement a control signal "Wait" for the decoder for loading data into the serializer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dipakkumar Gandhi
Patent Examiner